

REMARKS

This Amendment responds to the Final Office Action mailed July 25, 2007 in the above-identified application. The foregoing amendments do not raise new issues or require extensive consideration. In particular, the limitations of claim 26 are incorporated into amended claim 1. Accordingly, entry of the Amendment and allowance of the application are respectfully requested.

Claims 1-8 and 25-27 were previously pending in the application. Claims 9-24 were previously withdrawn from consideration and canceled. By this Amendment, claim 1 has been amended to incorporate the limitations of claim 26, and claim 26 has been canceled without prejudice or disclaimer. Accordingly, claims 1-8, 25 and 27 are currently pending, with claim 1 being the sole independent claim.

The Examiner's courtesy in conducting a telephone interview with inventor John Hayden and attorney William R. McClellan on October 24, 2007 is acknowledged with appreciation. During the telephone interview, the distinctions between Applicant's claim 1 and the cited Heath patent were discussed. The Applicant suggested a proposed amendment in which the limitations of claim 26 are incorporated into claim 1. The Examiner indicated that the proposed amendment overcame the rejection based on Heath.

The Examiner has rejected claims 1-3, 7 and 25-27 under 35 U.S.C. §102(b) as anticipated by Heath et al. (US 4,901,234). Claims 4-6 and 8 are rejected under 35 U.S.C. §103(a) as unpatentable over Heath et al. in view of Bowes et al. (US 5,655,151). The rejections are respectfully traversed in view of the amended claims.

Heath discloses a computer system in which peripherals greater in number than the number of DMA channels provided in the system can all have DMA access. Some of the DMA channels are dedicated to certain ones of the peripherals, while others, termed "programmable" DMA channels, are shared by remaining ones of the peripherals (Abstract). A DMA controller 12 is coupled to a system bus 26 and to a family bus 25 (Fig. 1). The details of DMA controller 12 are shown in Fig. 6 of Heath.

Amended claim 1 is directed to a DMA controller comprising, in part, at least one peripheral DMA channel, at least one memory DMA stream, first and second address computation units, first and second memory pipelines and a multiplexer. The first and second address computation units compute updated memory addresses for DMA transfers, wherein the first and second address computation units generate addresses at the same time to permit DMA transfer of data from one memory space to another memory space on the first and second memory access buses.

The Examiner asserts that Heath teaches a DMA controller wherein first and second address computation units generate addresses at the same time to permit DMA transfer of data from one memory space to another memory space on first and second memory access buses. The Examiner cites Heath, Fig. 6, elements 52, and col. 5, lines 51-55 as teaching first and second address computation units as claimed. Applicant must respectfully disagree. Heath contains no disclosure or suggestion that DMA controllers 52 shown in Fig. 6 contain address computation units.

Even assuming for the sake of argument that DMA controllers 52 contain address computation units, Heath teaches that the DMA controllers 52 are cascade-connected using NOR gates 53 (col. 5, lines 49-55). As shown in Fig. 6 of Heath, the HRQ output of the lower DMA controller is connected to the DREQ 0 input of the upper DMA controller, and the DACK 0 output of the upper DMA controller is connected to the HLD A input of the lower DMA controller. The cascade-connected DMA controllers permit eight DMA request inputs to the DMA controller. One of the COMPARE 0 - COMPARE 7 inputs is active (col. 5, lines 41-48). Only the upper DMA controller in Fig. 6 has an output to CPU 10. It appears that the two DMA controllers are cascade connected to function as a single DMA controller having eight request inputs. Heath contains no teaching or even a suggestion that the two DMA controllers 52 generate memory addresses at the same time. For at least these reasons, Heath does not disclose or suggest the DMA controller as defined by amended claim 1, and withdrawal of the rejection is respectfully requested.

Claims 2-8, 25 and 27 depend from claim 1 and are patentable over the cited references for at least the same reasons as claim 1.

Based upon the above discussion, entry of the Amendment and allowance of the application are respectfully requested.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Dated: October 25, 2007

Respectfully submitted,

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